

Fabrication and thermal characterization of silicon membranes for integrated thermoelectric converters

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In this talk, we report on the CMOS-compatible fabrication process of ultrathin silicon membranes (60 nm) from Silicon-on-Insulator (SOI) wafers. Additionally, the membranes are periodically perforated at deca-nanometer scale in order to reduce drastically thermal transport with low impact on the electrical conductivity in a so-called phonon-engineering approach [1]. As shown on figure 1, the process enables the fabrication of a wide variety of MEMS devices that can be used for: i) Thermal characterization by means of electro-thermal measurements [2], ii) Raman thermometry measurements of thermal conductivity [3], iii) Scanning Thermal Microscopy (SThM) study of thermal transport [4] and iv) integration as thermoelectric material in energy harvesting demonstrator [5].

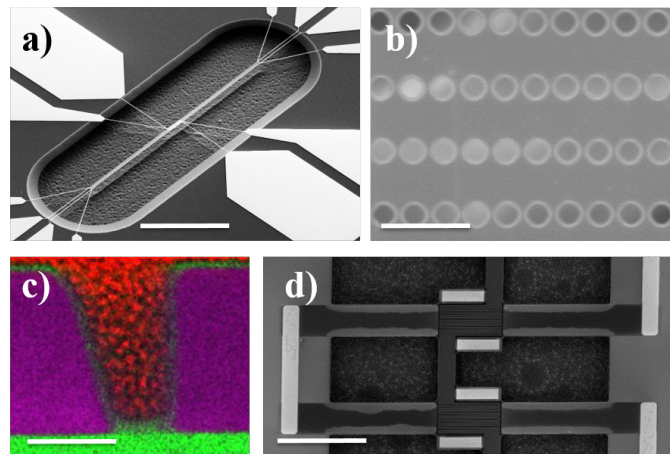


Figure 1: (a) Suspended membrane equipped for electro-thermal characterization (scale 60 μm). (b) Scanning Electron Micrograph of the surface nano-patterns (scale 250 nm). (c) Transmission Electron Micrograph of a hole pattern before membrane suspension (scale 40 nm). (d) Demonstrator of two thin-film thermopiles (scale 10 μm).

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