Chip Temperature Fields computed by Multi-Scale FEM Modelling and probed by Scanning Thermal Microscopy

A. Pic[a,b*], R. Prieto[a,c,d], S. Gallois-Garreignot[a], J.-P. Colonna[c] and P.-O. Chapuis[b]

a. STMicroelectronics, 850 Rue Jean Monnet, 38920 Crolles, France
b. Univ. Lyon, CNRS, INSA-Lyon, Université Claude Bernard
c. Univ. Grenoble Alpes, F-38000 Grenoble France CEA, LETI, MINATEC Campus, F-38054 Grenoble, France
d. Univ. Grenoble Alpes, G2Elab, F-38000 Grenoble, France CNRS, G2Elab, F-38000 Grenoble, France

* axel.pic@st.com & axel.pic@insa-lyon.fr

Heat dissipation is one of the main challenges faced by microelectronics due to the increase of integration density. For applications involving the Silicon-On-Insulator (SOI) technology based on a very thin silicon layer and imagers with high sensitivity to temperature spatial variations, accurate thermal characterizations with reliable temperature measurements are needed to quantify thermal performances at the device and package levels [1-2]. In this work, a 3D Hybrid Bonding (HB) assembly designed to highlight the heat dissipation issues is studied by means Finite Element Modelling (FEM). Experimental investigations of the HB assembly by successive means of resistive thermometry and Scanning Thermal Microscopy (SThM) allow feeding the model with accurate parameters and determining the full temperature field.

The test device designed to investigate the thermal behavior of the HB assembly [3] is made of two chips bonded by means of HB and involves materials typically used in microelectronics such as silicon bulk, oxides, nitrides and copper for interconnections. Four metal levels are considered - two in the bottom chip and two in the top one -, which all lay on top of a silicon die and a printed circuit board: the device is therefore a simplified version of more advanced chips. In the bottom metal level an electrical resistance is used to generate heat by Joule dissipation. The power dissipated represents that which would be generated in the integrated circuit (IC) of a real device.

The temperature in the chip is determined by means of numerical FEM studies at two different scales: the one of the heater and that of the whole package. However, some key parameters linked to the heat sink and the dissipation to ambient are needed. Embedded electro-thermal sensors made of resistive serpentines (12x12 μm^2) located in highest metal level of the chip [4] allow determining them. Once the full temperature field is computed, SThM, a surface mapping technique based on atomic force microscopy, is performed on the chip surface to validate the numerical results. Two probes are used successively: the Wollaston and Pd tips. It is important to mention that the SThM sensors need also to be simulated through FEM in order to get quantitative data from the measurements, as they modify the heat dissipation channels when set in contact with the HB assembly.

The results show an interesting match of the experimental SThM data and the computed ones. SThM is particularly useful when optical techniques cannot be used. The mid-term goal of the project is to develop a library of effective parameters for the FEM simulation tools and validate simulation methods for such issue. This will allow predictions of thermal behaviors of more complex electronic stacks with improved accuracy.

References

[1] G. Garegnani et al, Microelec. Rel. 63, 90, 2016
[2] D.L. Lin et al, IEEE Trans. Elect. Dev. 57, 2010
[3] C. Sart et al, Proceedings of ESTC6, 2016
[4] R. Prieto et al, Proceedings of THERMINIC, 2016
[5] M. Nonnenmacher et al, Appl. Phys. Lett. 61, 168, 1992
[6] A. Assy, PhD Thesis, INSA Lyon, 2015

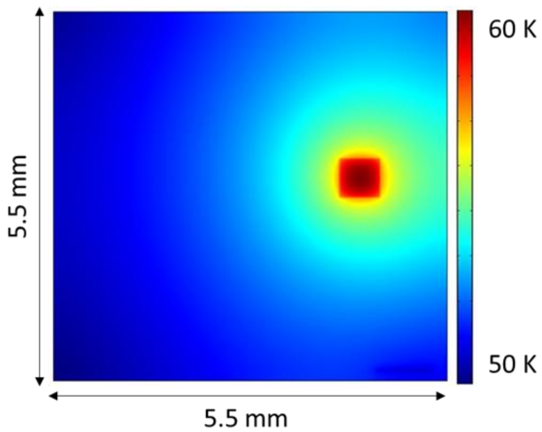

Figure: Temperature rise of the chip surface calculated by FEM