Design and development of 3D arrays of coupled Quantum Dots in SOI CMOS technology

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Silicon-based spin qubits are an extremely attractive option for large-scale quantum computing owing to their relatively long spin coherence time, as well as their potential for leveraging the technological maturity of the IC manufacturing industry towards mass fabrication. Thus, the development of various structures and array of Quantum Dots (QDs) have been studied, and scaling the number of qubits is necessary for the next challenge [1-3]. In order to demonstrate a full-scale universal quantum computer, error correction code should be developed, and it can be realized in 2D arrays of QDs [4]. Thus, recent proposals of 2D arrays are offered, using crossbar addressing of the QDs and the tunnel junctions in order to reduce the number of I/Os [5,6]. However, the proper balance between tunability, integration density, cross-talk and variability management is still being evaluated.

Here we suggest an array with a 3D elementary cell as shown in Fig. 1(a). Fig. 1(b) shows the structure of 3D elementary cell composed of five dots, which are one measurement (M), four data (D), and one sensing (S) dots in two layers. In the top layer, M dots are coupled to the D dots in 2D array to implement a quantum error correction. The localization and coupling of electrons can be controlled with tuning tunnel junction between M and D dots by applying voltage to the plug Gates above dots (Fig. 1(c)). Moreover, S dots are coupled to the M dots by a silicon pillar, which can be controlled with line/column addressing by wrapping Gates (Gate-All-Around geometry). Thus the S dots can be used either to load electrons into the QDs in the top layer, or to sense spin-related charge events occurring in the top dots (Fig. 1(d)). Then our current work aims at paving the way for the realization of the full structure by validating the dimensions and feasibility of the main technological modules (patterning, epitaxial growth, bonding, etc.)

[1] D.M. Zajac et al., Resonantly driven CNOT gate for electron spins, Science, 359, 439-442 (2018)

[2] R. Maurand et al., A CMOS silicon spin qubit, Nat. Commun., 7, 13575 (2016)

[3] T.F. Watson et al., A programmable two-qubit quantum processor in silicon, Nature, 555, 633-637 (2018)

[4] A.G. Fowler, Surface codes: Towards practical large-scale quantum computation, Phys. Rev. A, 86, 032324 (2012)
[5] M. Veldhorst et al., Silicon CMOS architecture for a spin-based quantum computer, Nat. Commun., 8:1766 (2017)
[6] R. Li et al., A Crossbar Network for Silicon Quantum Dot Qubits, arXiv:1711.03807 (2017)



Fig. 1(a) The full structure of an array with 3D elementary cell, (b) the structure of 3D elementary cell, (c) top view and (d) cross-section of 3D elementary cell.