Self-heating in nanostructures: a quantum mechanical view

Mathieu Luisier[a*], Reto Rhyner[b], and Aron Szabo[a]

a. Integrated Systems Laboratory, ETH Zurich, 8092 Zurich, Switzerland
b. Synopsys Switzerland LLC, Thurgauerstrasse 40, 8059 Zurich, Switzerland

* mluisier@iis.ee.ethz.ch

Over the years, driven by Moore's scaling law, the active dimensions of electronic devices have been pushed down towards their ultimate limit. This especially concerns Silicon-based logic switches, for which the supply voltage has not been reduced as fast as their size. As a consequence, the amount of power dissipated per area has kept increasing from one generation of transistors to the other, reaching nowadays alarming values [1]. To stop this trend, it is important to first understand what physical mechanisms govern power and heat dissipation in nanostructures, how much self-heating occurs at the nanoscale, and how this effect could be potentially circumvented by adopting novel device geometries or by replacing Si with another material.

Technology computer aided design (TCAD) can help address these issues, provided that advanced simulation tools based on suitable physical models exist. When the device dimensions do not exceed a few nanometers anymore, quantum mechanical phenomena, e.g. energy quantization, confinement, or tunneling, start to play a fundamental role. To produce accurate results or predict the performance of not-yet-fabricated components, they must be properly accounted for, not only to describe electron transport, but also the propagation of heat through a given medium. Here, a modeling approach that fulfills these requirements will be presented. It relies on coupled electron and phonon transport at the quantum mechanical level. The material properties are expressed either in an empirical (tight-binding for electrons, valence-force-field for phonons) or in a fully *ab-initio* (density-functional theory) basis. Exemplary results of electro-thermal transport simulations are shown in Fig. 1 for a Si nanowire transistor. The case of self-heating in 2-D materials, in particular MoS_2, will also be discussed.

[1] E. Pop, S. Sinha, and K. E. Goodson, Heat Generation and Transport in Nanometer-Scale Transistors, Proc. IEEE **94**, 1587 (2006).
[2] R. Rhyner and M. Luisier, Atomistic modeling of coupled electron-phonon transport in nanowire transistors, Phys. Rev. B **89**, 235311 (2014).

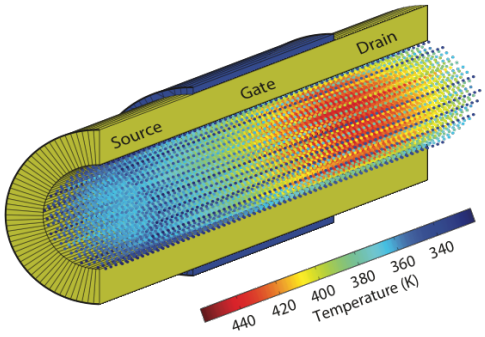

Figure 1: Atomically-resolved temperature distribution inside a Si gate-all-around nanowire transistor with a diameter d=3 nm. A significant temperature increase close to the drain side of the device can be observed.